Improved Power Rating of Cascaded H-Bridge Multilevel Inverter

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***Abstract*—This paper presents a simulation of 5-level Cascaded Diode Clamped Half Bridge (CDCHB) Inverter using Hybrid Level-shifted and Phase-shifted (HLP) Sinusoidal Pulse Width Modulation (SPWM) technique. The output voltage, output current and voltage across each device, and the THD of the CDCHB inverter are obtained. Further, the paper aims to perform a comparison between 5-level CDCHB inverter with Cascaded H-Bridge (CHB) inverter. The comparison is done on the basis of the peak inverse voltage of each device, output power and the THD obtained with both the inverters. Simulations are done in MATLAB Simulink and results obtained are shown.**

Keywords*—Total Harmonic Distortion (THD), Cascaded H-Bridge (CHB), Cascaded Diode Clamped Half Bridge (CDCHB), Hybrid Level-shifted and Phase-shifted (HLP), Sinusoidal Pulse Width Modulation (SPWM).

I. INTRODUCTION

The power conversion systems for large renewable energy stations are facing a great challenge today as Battery Energy Storage Systems (BESS), PV cells and all other renewable energy sources output approaches in MWs, which demand three phase multi-level inverters. Medium voltage applications include high power motor drives, high power uninterruptable power supplies (UPSs), flexible ac transmission systems (FACTs). Neutral (diode) clamped converters (NCCs), capacitor clamped converters (FCs), and cascaded H-Bridge converters (CHBs) are the typical multi-level converters [1-2].

The CHB Multi Level Converter is recognized for its modular structure, fault toleration ability, and high-reliability. It is used in high voltage applications, because this circuit requires the least number of components to synthesize the same number of voltage levels. It provides definite dc links to which dc source strings are connected, and it easily reaches medium voltage. Also, its hardware implementation is simple, employs simple switching logic and has easy maintenance. Although, since each H-bridge cell has its independent dc source system with its own power point, there is a distinctive power imbalance between the cells. If this imbalance is not taken into deliberation in the control scheme, the dc link voltages will drift. CHB multilevel converters are used as converters in ac motor drives, active power filters, and high power conditioning. These can also be used as pulse-width modulation (PWM) rectifiers. However, the need for isolated dc supplies for each H Bridge unit makes it costly [3].

In this paper, a five level Cascaded Diode Clamped Half Bridge (CDCHB) inverter is analyzed. The output voltage stress, output power and voltage stress across each switch is studied. The paper evaluates the performance of five level CDCHB inverter. A cascaded h-bridge (CHB) inverter is simulated and their performances are compared. In order to prove the proposed advantages, results are provided and comparison is done between the two.

II. 5-LEVEL CASCADED H-BRIDGE INVERTER

Fig. 1 shows a 5-level CHB inverter. CHB multilevel converters first appeared in 1988, matured during 1990s, and gained attention after 1997 [4]. CHB multilevel converters are characterized by cascade connection of isolated series connected full bridge modular chopper-cells or H-bridge cells to form each arm, which brings flexibility to circuit. In each arm there are two full bridge cells connected in series. Each cell has four switches. The pattern for providing the switching signals is shown. Based on multicarrier level and phase shifted sinusoidal pulse width modulation, switching pulses are generated to produce voltage levels of $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$.

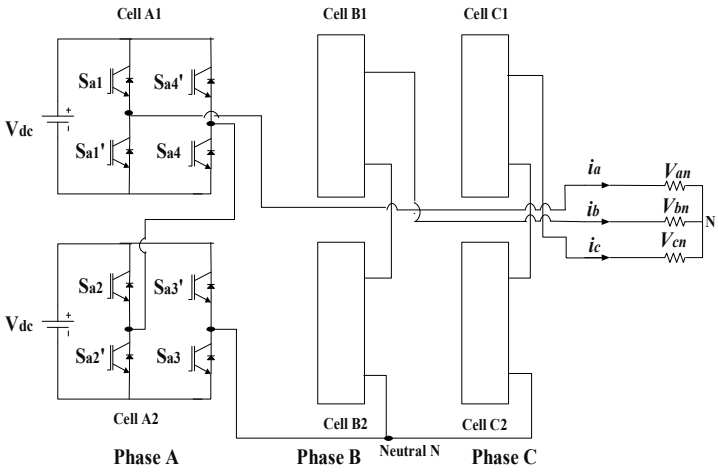

Fig. 1 5-level Cascaded H-Bridge inverter.

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Level shifted pulse width modulation is used for five level CHB inverter, where the four triangular carrier signals, all having the same frequency and peak-to-peak amplitudes, are vertically disposed such that the bands they occupy are contiguous and these signals are compared with single sinusoidal modulating signal for phase-*a* [5,6].

The number of levels (m) in phase voltage with n number of H-bridge cells per phase leg can be found out with the equation:

$$m= 2n+1$$

If the input voltage is V_{dc} , then the voltage stress across each switch is also V_{dc}. The output apparent power is $3\times V_{orms} \times I_{orms} = S_{o.}$

III. 5-LEVEL CASCADED DIODE CLAMPED HALF BRIDGE INVERTER

Cascaded Diode Clamped Half-Bridge (CDCHB) inverters are characterized by series connected half-bridge modules instead of full bridge ones. These converters can be used as an alternative to the conventional CHB inverters. Pairs of half bridge modules are connected in series. Each cell has 4 switches connected in series, with a different switching scheme. The circuit diagram is shown in fig. 2.

If the input voltage here is V_{dc}, then the voltage stress across each switch is also (V_{dc}/2). For the same voltage, the voltage stress across each device is reduced to half times of the previous case. The output apparent power is = $3\times V'_{orms} \times I'_{orms} = S'_o$. S'_o is greater than two times of S_o. Therefore for the same voltage stress across each switch, V_{dc}, the input voltage in cascaded half bridge inverter can be increased to $2V_{dc}$. The advantage is that this proposed topology can be used with high voltage renewable sources of energy. Since the power handling capability in this case is doubled, it can also be used with modern day high MVA loads.

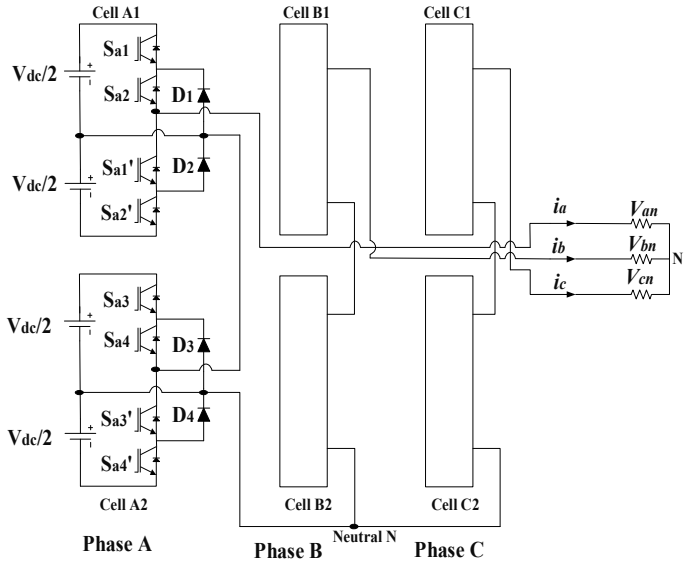

Fig. 2 5-level cascaded diode clamped half bridge inverter.

Moreover the output current waveforms are perfectly sinusoidal, which is a prime requirement for ac loads connected to inverters. All these features make this proposed topology better than CHB inverter.

IV. HYBRID PWM SWITCHING STRATEGY

The Hybrid Level-shifted and Phase-shifted (HLP) Sinusoidal Pulse Width Modulation (SPWM) scheme is discussed considering that each phase is cascaded with two cells only for better perception. The HLP-SPWM scheme and the switching patterns given for phase-*a* (cell A_1 and A_2) with modulating signals m_{a1} and m_{a2} respectively are shown in Fig. 3. Because of symmetry in the three phases, attention is paid only to phase-*a*. For each cell, a pair of triangular carriers is equally spaced in a positive and negative band. For subsequent cell, a phase delay of $360^0/n$ is maintained between each pair of carriers as shown in Fig, where '*n*' is cascaded number of cells in a phase. In Fig. 3, cr_1 and cr_2 represents the triangular carriers to generate firing pulses for switches S_{a1} and S_{a2} respectively in cell 'A_1' with reference to modulating signal m_{a1}. So cr_1 and cr_2 are level shifted to each other. Whereas carrier cr_3 and cr_4 are the other pair of triangular carriers (sketched in dotted lines) and these two carriers are phase shifted with respect to cr_1 and cr_2 to generate firing pulses for switches S_{a3} and S_{a4} respectively in cell 2 with respect to modulating signal m_{a2}. So the carriers within the cells are level shifted, whereas carrier for two different cells are phase shifted with respect to the first cell carriers.

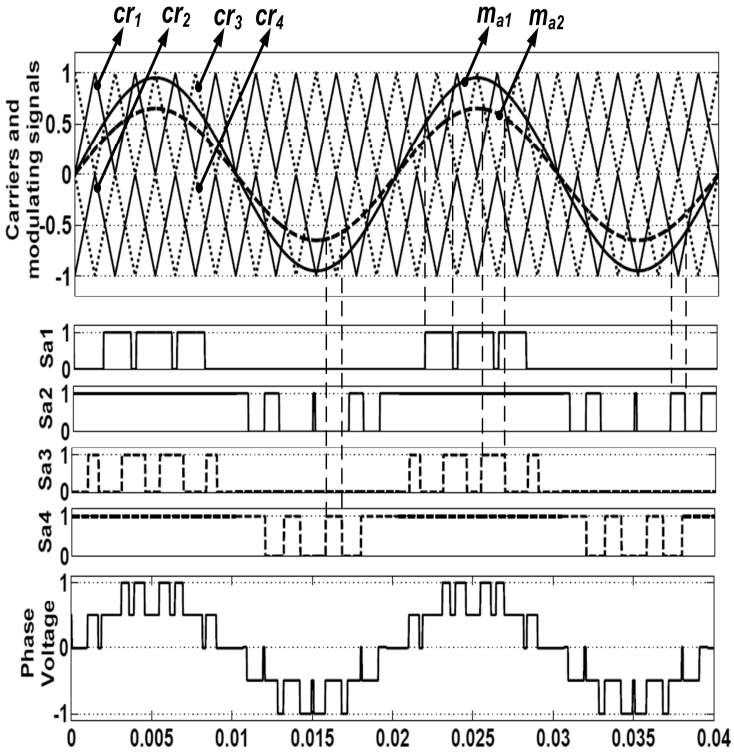

Fig. 3 PWM scheme for 5-level cascaded diode clamped half bridge inverter.

Firing pulses for switches S_{a1}' and S_{a2}' can be obtained by 'Not' operation of S_{a1} and S_{a2}. S_{a3}' and S_{a4}' can be obtained by 'Not' operation of S_{a3} and S_{a4}. From fig, it can also be observed that the alignment of obtained voltages in both the cells of phase-*a* gives rise to form five levels in phase voltage at the ac side of the converter. All the three phases are simultaneously operated to provide the transformer less grid connected renewable energy generation system where the line voltage consists of nine level with less THD [6-8].

TABLE I. SWITCHING SIGNALS FOR SWITCHES IN PHASE-*a* OF THE INVERTERS

	CHB Inverter	**CDCHB Inverter**
S1	S_{a1}	S_{a1}
S2	S_{a1}'	S_{a2}
S3	S_{a4}'	S_{a1}'
S4	S_{a4}	S_{a2}'
S5	S_{a2}	S_{a3}
S6	S_{a2}'	S_{a4}
S7	S_{a3}'	S_{a3}'
S8	S_{a3}	S_{a4}'

V. SIMULATION RESULTS

This section presents the simulation results for the two inverters and comparison is done between them to prove the above statements and evaluate the validity of the proposed topology. Simulations are done in the MATLAB Simulink environment. RL load is used in the ac side. The design parameters for the simulation of both the inverters are tabulated in Table II.

TABLE II. DESIGN PARAMETERS FOR THE SIMULATION

Parameters	**5-Level CHB Inverter**	**5-Level CDCHB Inverter**
Number of switches in each cell	4	4
DC Input Voltage	4300 V	4300×2=8600 V
Modulation Index	0.95	0.95
Switching Frequency	3000 Hz	3000 Hz
RL Load	P= 0.8MW Q= 0.6 MVAR	P= 1.6 MW Q= 1.2 MVAR

It is observed that for CHB inverter, the I_{dc} = 32.1 A and peavalue of phase voltage, V_{opeak} = 8600 V.

While that for CDCHB inverter, I_{dc} = 58.47 A and peak value of phase voltage, V_{opeak} = 8600 V.

A. *Study of output power and their comparison*

In the CHB inverter,

RMS value of output voltage, V_{orms} = 6039 V.
RMS value of output current, I_{orms} = 47.76 A
Therefore output apparent power $S_o = 3\times V_{orms}\times I_{orms}$ = 0.865 MVA

Whereas in CDCHB inverter,

RMS value of output voltage, V'_{orms} = 6393 V.
RMS value of output current, I'_{orms} = 100 A
Therefore output apparent power $S'_o = 3\times V'_{orms}\times I'_{orms}$ = 1.9179 MVA

So it is verified that, the power rating of the ac load connected to the inverter becomes two fold.

B. *Study of PIV across devices and their comparison*

Fig. 9 and Fig. 15 show the PIV across each switch for both the cases. It is clearly seen that the device voltage stressing remains same though the input dc voltage for the cascaded half bridge inverter is doubled. This allows the topology to be used with high voltages without causing damage to the IGBT switches.

C. *Study of the output voltage and current waveforms*

The output phase voltages of the two inverters are shown in Fig. 4, Fig. 5, Fig. 6, Fig. 10, Fig. 11, and Fig. 12. The phase voltages of both these topologies have 5-levels. The current waveforms are purely sinusoidal. I_b is lagging and I_c is leading to I_a in nature, shown in Fig. 7 and Fig. 13.

D. *Study of current and voltage THD and their comparison*

Fig.8. and fig.14 show the voltage THDs of the two inverter topologies respectively.

For CHB inverter,

Current THD= 0.7489 % and Voltage THD= 27.19 %

For CDCHB inverter,

Current THD= 0.69 % and Voltage THD= 22.38 %

Therefore the results state that THD is also minimized for the CDCHB inverter topology. For calculating THD all the harmonics is considered. If the number of level will increase THD will also improve. For CDCHB inverter the THD shown in fig. 14. This THD can be improved to the permissible range by increasing the number of level of cascaded half bridge inverter. It is observed the peak value of fundamental voltage is 8518 V and for CHB it is only 8169 V while both inverter have same peak output voltage, which shows the cascaded half bridge inverter has capability to eliminate higher order harmonics. Also the power rating of each cell of CDCHB inverter is more than CHB inverter. Table. III displays the results obtained for CHB and CDCHB inverters.

Results for CHB inverter

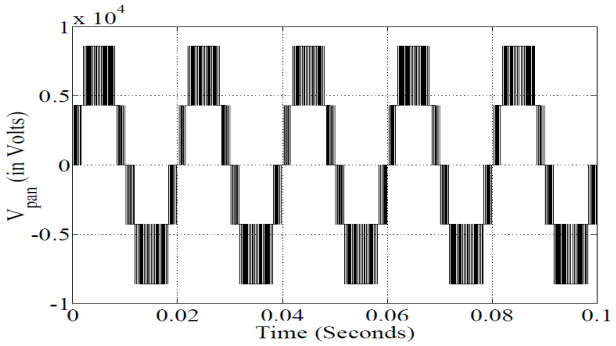

Fig. 4. Voltage of phase-a with respect to neutral.

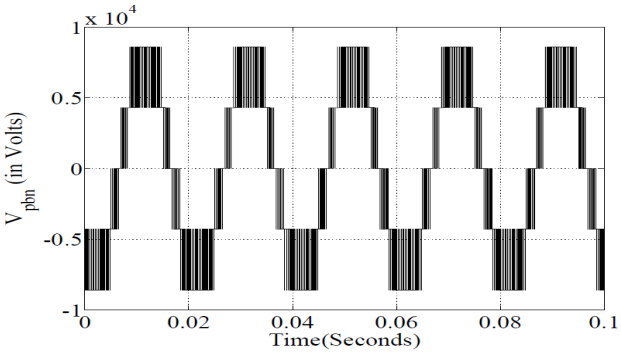

Fig. 5. Voltage of phase-b with respect to neutral.

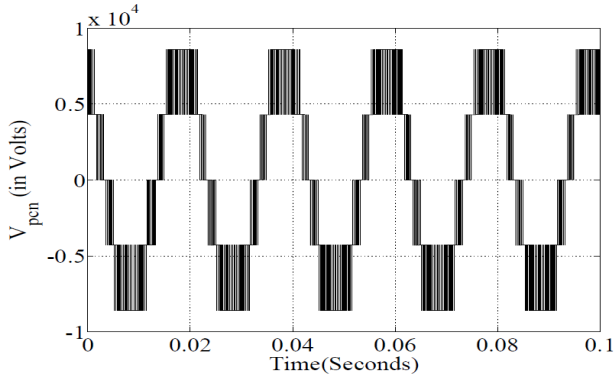

Fig. 6. Voltage of phase-c with respect to neutral.

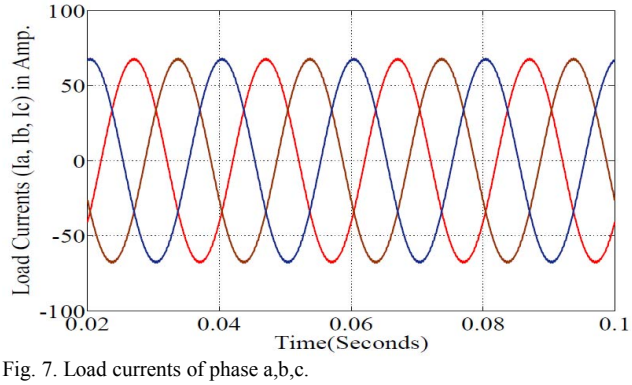

Fig. 7. Load currents of phase a,b,c.

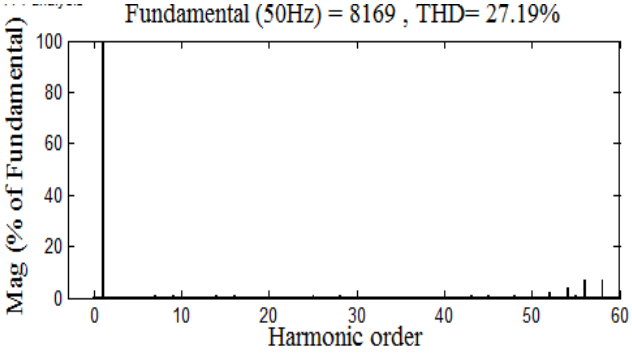

Fig. 8. Phase voltage THD with respect to fundamental.

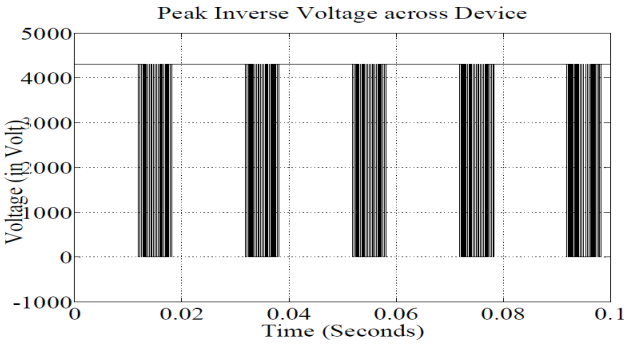

Fig. 9. Peak Inverse Voltage across device.

Results for CDCHB inverter

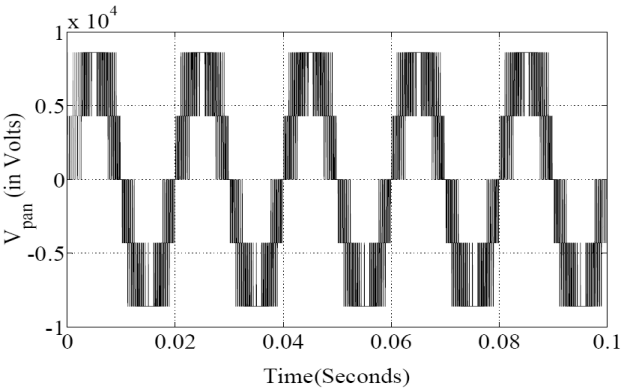

Fig. 10. Voltage of phase-a with respect to neutral.

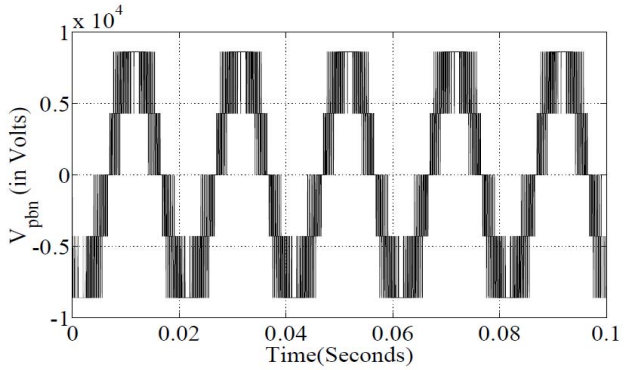

Fig. 11. Voltage of phase-b with respect to neutral.

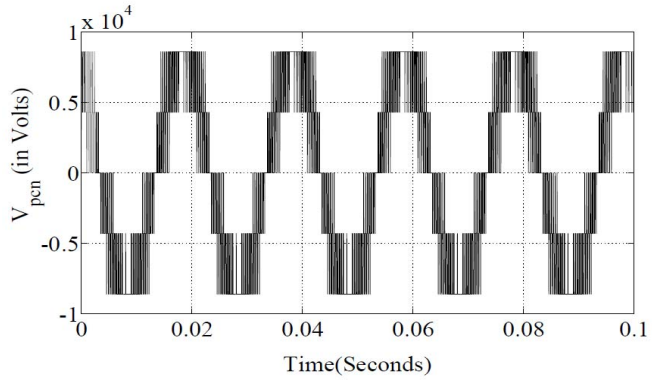

Fig. 12. Voltage of phase-c with respect to neutral.

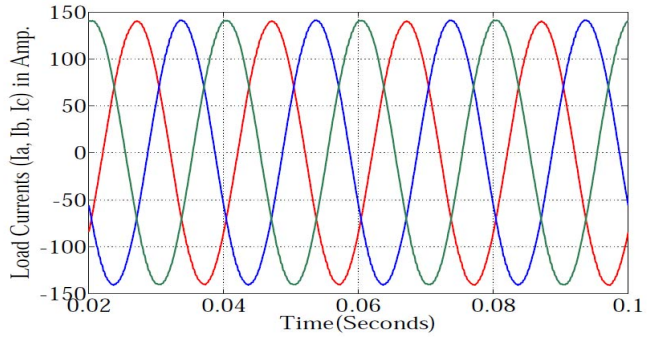

Fig. 13. Load currents of phase a,b,c.

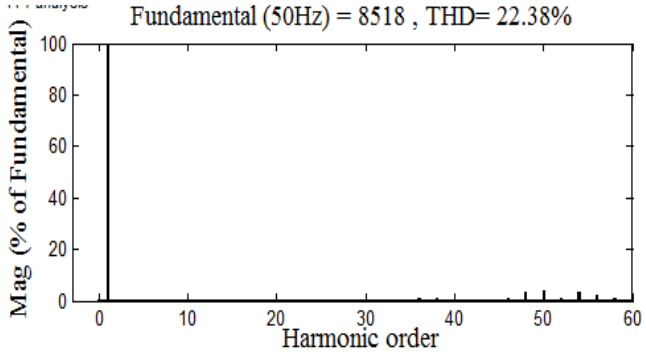

Fig. 14. Phase voltage THD with respect to fundamental.

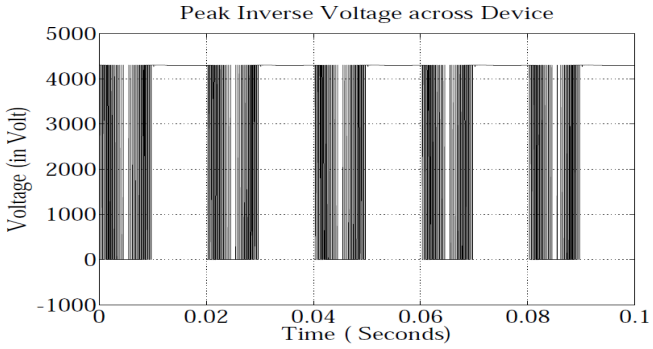

Fig. 15. Peak Inverse Voltage across device.

TABLE III. COMPARATIVE RESULTS

Properties	5-Level CHB Inverter	5-Level CDCHB Inverter
Peak inverse voltage (PIV)	4300 V	4300 V
Output Voltages V_{orms} , V'_{orms}	6039 V	6393 V
Output Currents I_{orms} , I'_{orms}	47.76 A	100 A
Output MVA	0.865 MVA	1.9179 MVA
Current THD	0.75 %	0.69 %
Voltage THD	27.19 %	22.38%

VI. CONCLUSION

In this paper, HLP-SPWM scheme uses both level shifted as well as phase shifted technique and it is applied for 5-level CDCHB inverter. Its performance is compared with a 5-level CHB inverter. The comparison is done in the following aspects: number of switches, input voltage, peak inverse voltage, output power, current and voltage THD. Voltage stress across each switch in CDCHB is found to be same as in CHB even if the applied input voltage is doubled, and power rating of each cell is also doubled in CDCHB than CHB. THD is improved in CDCHB but THD can be further improved by increasing the number of level of output voltage.

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